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Sheet 1 of 3

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		DOCKET NO. AL-212 Cont.	APPLN. NO. 10/643,276
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANTS		APPLICANTS Chong H. Lee et al.	CONF. NO. 4060
		FILING DATE August 18, 2003	GROUP ART UNIT 2819

U.S. PATENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
<i>hl</i>	4,972,470	11/20/1990	Farago	713	192	
	5,379,382	1/3/1995	Work et al.	710	63	
	5,402,014	3/28/1995	Ziklik et al.	326	37	
	5,457,784	10/10/1995	Wells et al.	710	9	
	5,557,219	9/17/96	Norwood et al.	326	49	
	5,574,388	11/12/1996	Barbier et al.	326	41	
	5,689,195	11/18/1997	Cliff et al.	326	41	
	6,005,412	12/21/1999	Ranjan et al.	326	63	
	6,038,400	3/14/2000	Bell et al.	710	11	
	6,122,747	9/19/2000	Krening et al.	713	323	
	6,128,673	10/3/2000	Aronson et al.	710	22	
	6,131,125	10/10/2000	Rostoker et al.	709	250	
	6,145,020	11/7/2000	Barnett	710	8	
<i>hl</i>	6,185,641	2/6/2001	Dunnihoo	710	56	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
<i>hl</i>	2 323 000	9/9/1998	GB	G06F	13/38		
<i>hl</i>	1 248 372	10/9/2002	EP	H03K	19/177		

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J. Dan *CT*

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90/14/04

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL	
<u>W</u>	Bursky, Dave, "Higher-Throughput DSP Chips Take on Complex Applications," Electronic Design, May 25, 1988.
<u>1</u>	Leonard, Milt, "Digital System Design (Mastering New Devices and Design Methodologies)," Electronic Design, Vol. 37, No. 1, p. 88-95, January 12, 1989.
	Abe, Koki et al., "A Microcomputer Implementation of PLA Function and Its Use in a Laboratory Dealing with Arithmetic Algorithms," IEEE Transactions on Education, Vol. 32, No. 2, pp. 129-138, May 1989.
	Clark, Barry M., "Improve Reliability by Rigging PC Boards for In-Circuit Programming," EDN, Vol. 37, No. 8, p. 135-140 April 9, 1992.
	Gallant, John, "High-Density PLDs," EDN, Vol. 40, No. 6, p. 31-35, March 16, 1995.
	Bursky, Dave, "Lower-Power and Faster Devices Tackle Multimedia Needs," Electronic Design, Vol. 44, No. 9, p. 90-96, May 1, 1996.
	Press Release, Lucent Technologies, Lucent Technologies ORCA Series to be Supported by Synopsys' FPGA Express (June 3, 1996).
	Press Release, Lucent Technologies, Lucent Announces Plans for 225,000 Gate FPGAs with System Level Functions and Field Programmable System Chips (October 21, 1996).
	Press Release, Lucent Technologies, Lucent Technologies' New Series 3 Family of FPGAs Offers System-Level Features for Faster Development (March 3, 1998).
	Press Release, Lucent Technologies, Lucent Technologies, Combines FPGA, Standard-Cell Logic on Single Silicon Chip for High Performance, Flexibility (May 11, 1998).
	"Atmel Corp. - History & Debt Report," Atmel Corp., - History and Debt Report, December 26, 1998.
	Dipert, Brian, "The Best (or Worst?) of Both Worlds (Hybrid Application-Specific ICs/Programmable Logic Devices)," EDN, Vol. 44, No. 23, P. 139, November 1, 1999.
	"Lucent Technologies Boosts Field-Programmable Gate Array -FPGA Performance for Broadband Communications Applications," Business Wire, p. 1, July 3, 2000.
	"QuickFC-PCI Interface," APPNote #54, QuickLogic Customer Engineering, August 30, 2000.
	Bursky, Dave, "FPGA Combines Multiple Serial Interfaces and Logic," Electronic Design, Vol. 48, No. 20, p. 74, October 2, 2000.
	Press Release, Actel Corporation, Actel Announces Five Productivity Enhancing IP Cores For SX, SX-A And eX Devices (November 17, 2000).
	Souza, Crista, "Lucent FPSCs Aid 10-Gbit Ethernet Design," Electronic Buyers' News, p. 41, November 20, 2000.
<u>W</u>	"Cypress to Mix Programmable Logic, High-Speed Serial I/O in New Chip Series," ComSoc News, December 18, 2000.

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<i>W</i>	"Cypress Interface to Bypass Backplane Bottlenecks – Serial Devices Address Bus Problems Such as Noise, Speed, and Scalability," EBN, p. 39, January 1, 2001.
	"What's Making Waves in the Market," Fiber Optics News, Vol. 21, No. 2, January 8, 2001.
	"ORCA® ORT8850 Field-Programmable System Chip (FPSC) Eight-Channel x 850 Mbits/s Backplane Transceiver," Product Brief, Agere Systems, July 2001.
	"ORCA® ORT8850 Field-Programmable System Chip (FPSC) Eight-Channel x 850 Mbits/s Backplane Transceiver," Data Sheet, Agere Systems, August 2001.
	Moore, Michael, "Speeding Up Your Backplane," Circuit Cellar Online, pp. 1-6, November 2001.
<i>W</i>	Gomes, Luis, "Introducing Programmable Logic Devices into Digital Design," IEEE, pp. 73-74, 2001.

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Daw CE

DATE CONSIDERED

10/14/04

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